IN THE CLAIMS:

Please cancel claims 8, 18, 62, 72, 90-101, and 110 without prejudice or disclaimer as to the subject matter contained therein.

Please amend the claims as shown below in the listing of claims.

1. (Currently amended) A crossbar switch, comprising:

a plurality of input sorting units, each input sorting unit capable of receiving from a respective device an access request to any one of a plurality of physical memory devices;

a plurality of merge and interleave units, each merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device;

wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of generating a composite request priority from a plurality of characteristics of the access requests and a plurality of operational characteristics;

a priority compare circuit capable of selecting one access request;

a request multiplexer controlled by the priority compare circuit to output the selected access request;

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

2. (Original) The crossbar switch of claim 1, further comprising a plurality of translation circuits and wherein each of the input sorting units receives the access requests through a respective one of the translation circuits.

3. (Original) The crossbar switch of claim 2, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

4. (Original) The crossbar switch of claim 1, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

5. (Original) The crossbar switch of claim 4, wherein the buffer is a first-in, first-out queue.

6. (Original) The crossbar switch of claim 4, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

7. (Currently amended) The crossbar switch of claim 1, wherein each merge and interleave unit further includes:

[a] the priority generator for each input sorting unit being further capable of:

receiving [a] the plurality of characteristics for the access request received by the input sorting unit;

receiving [a] the plurality of operational characteristics; and

generating [a] the composite request priority from the characteristics of the access requests and the operational characteristics;

[a] the priority compare circuit being further capable of:

comparing the composite request priorities generated by the priority generators; and

selecting the one access request predicated on the comparison of the composite request priorities~~; and~~

~~a request multiplexer controlled by the priority compare circuit to output the selected access request~~.

8. (Cancelled)

9. (Original) The crossbar switch of claim 1, further comprising:

a plurality of read buffers capable of receiving and buffering read data from a respective one of the physical memory devices; and

a plurality of output management units capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

10. (Original) The crossbar switch of claim 1, further comprising a plurality of memory interfaces capable of receiving the selected access request from a respective one of the plurality of merge and interleave units and forwarding the selected access request to a respective one of the physical memory devices.

11. (Currently amended) A crossbar switch, comprising a plurality of arbitration and select units, each arbitration and select unit including:

a plurality of front ends, each front end comprising:

a translation circuit capable of processing an access request received from a respective device;

an input sorting unit capable of buffering and forwarding the processed access request;

an output management unit capable of receiving read data generated by the access request and forwarding the received read data to the respective device; and

a plurality of back ends, each back end comprising:

a merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests, and forwarding the selected request for implementation on a respective memory device;

wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of generating a composite request priority from a plurality of characteristics of the access requests and a plurality of received operational characteristics;

a priority compare circuit capable of selecting one access request;

a request multiplexer controlled by the priority compare circuit to output the selected access request.

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output; and

a read buffer capable of receiving, buffering, and forwarding read data received from the respective memory device to the output management unit of the front end that issued a previously selected access request that generated the read data.

12. (Original) The crossbar switch of claim 11, wherein each back end further comprises a memory interface through which the merge and interleave unit forwards the selected request.

13. (Original) The crossbar switch of claim 11, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective

device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

14. (Previously presented) The crossbar switch of claim 11, wherein each of the input sorting units includes a request buffer and is capable of buffering the access requests from its respective physical memory device.

15. (Previously presented) The crossbar switch of claim 14, wherein the request buffer is a first-in, first-out queue.

16. (Previously presented) The crossbar switch of claim 14, wherein each of the input sorting units is capable of stalling its respective device when its request buffer is full.

17. (Currently amended) The crossbar switch of claim 11, wherein each merge and interleave unit further includes:

[a] the priority generator for each input sorting unit being further capable of:

receiving [a] the plurality of characteristics for the access request received by the input sorting unit;

receiving [a] the plurality of operational characteristics; and

generating [a] the composite request priority from the characteristics of the access requests and the operational characteristics;

[a] the priority compare circuit being further capable of:

comparing the composite request priorities generated by the priority generators; and

selecting the one access request predicated on the comparison of the composite request priorities~~; and~~

~~a request multiplexer controlled by the priority compare circuit to output the selected access request~~.

18. (Cancelled)

19-54. (Cancelled)

55. (Currently amended) A crossbar switch, comprising a plurality of arbitration and select units, each arbitration and select unit including:

a plurality of front ends, each front end further including an input sorting unit capable of receiving from a respective device an access request to any one of a plurality of physical memory devices;

a plurality of back ends, each back end further including merge and interleave unit capable of arbitrating among competing access requests received from any of the input sorting units, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device;

wherein each merge and interleave unit includes:

a priority generator for each input sorting unit capable of generating a composite request priority from a plurality of characteristics of the access requests and a plurality of received operational characteristics;

a priority compare circuit capable of selecting one access request;

a request multiplexer controlled by the priority compare circuit to output the selected access request.

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

56. (Original) The crossbar switch of claim 55, wherein each front end further comprises a Glue logic unit and wherein each of the input sorting units receives the access requests through a respective one of the Glue logic units.

57. (Original) The crossbar switch of claim 56, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

58. (Original) The crossbar switch of claim 55, wherein each of the input sorting units includes a buffer and is capable of buffering the access requests from its respective physical memory device.

59. (Original) The crossbar switch of claim 58, wherein the buffer is a first-in, first-out queue.

60. (Original) The crossbar switch of claim 58, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

61. (Currently amended) The crossbar switch of claim 55, wherein each merge and interleave unit further includes:

[a] the priority generator for each input sorting unit being further capable of:

receiving [a] the plurality of characteristics for the access request received by the input sorting unit;

receiving [a] the plurality of operational characteristics; and

generating [a] the composite request priority from the characteristics of the access requests and the operational characteristics;

[a] the priority compare circuit being further capable of:

comparing the composite request priorities generated by the priority generators; and

selecting the one access request predicated on the comparison of the composite request priorities~~; and~~

~~a request multiplexer controlled by the priority compare circuit to output the selected access request~~.

62. (Cancelled)

63. (Original) The crossbar switch of claim 55, wherein:

each back end further includes a read buffer capable of receiving and buffering read data from a respective one of the physical memory devices; and

each front end further includes an output management unit capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

64. (Original) The crossbar switch of claim 55, wherein each back end further comprises a memory interface capable of receiving the selected access request from the merge and interleave unit and forwarding the selected access request to a respective one of the physical memory devices.

65. (Currently amended) A crossbar switch, comprising a plurality of arbitration and select units, each arbitration and select unit including:

a plurality of front ends, each front end comprising:

means for processing an access request received from a respective device;

means for buffering and forwarding the processed access request;

means for receiving read data generated by the access request and forwarding the received read data to the respective device; and

a plurality of back ends, each back end comprising:

means for arbitrating among competing access requests received from ~~any of the input sorting units~~ the means for processing an access

request, selecting one of the competing access requests, and forwarding the selected request for implementation on a respective memory device; and

means for receiving, buffering, and forwarding read data received from the respective memory device to the output management unit of the front end that issued a previously selected access request that generated the read data;

means for generating a composite request priority from a plurality of characteristics for the access requests and a plurality of operational characteristics;

means for selecting one access request; and

means for outputting the selected access request via a multiplexing means, the multiplexing means being controlled by the means for selecting the one access request.

means for storing programmable weights;

a decode unit receiving the selected request from the multiplexing means to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the storage means; and

means for combining register read data with request data for output.

66. (Original) The crossbar switch of claim 65, wherein each back end further comprises a memory interface through which the merge and interleave unit forwards the selected request.

67. (Original) The crossbar switch of claim 65, wherein each processing means is further capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

68. (Original) The crossbar switch of claim 65, wherein each of the processed access request buffering means includes a buffer and is capable of buffering the access requests from its respective physical memory device.

69. (Original) The crossbar switch of claim 68, wherein the buffer is a first-in, first-out queue.

70. (Original) The crossbar switch of claim 68, wherein each of the processed access request buffering means is capable of stalling its respective device when its buffer is full.

71. (Currently amended) The crossbar switch of claim 65, wherein each arbitration and selection ~~means~~ unit further includes:

means for receiving [a] the plurality of characteristics for the access request received by the input sorting unit, receiving [a] the plurality of operational characteristics, and generating [a] the composite request priority from the characteristics of the access requests and the operational characteristics;

means for comparing the composite request priorities generated by the priority generators, and selecting the one access request predicated on the comparison of the composite request priorities~~; and~~

~~means for multiplexing signals, the multiplexing means being controlled by the comparing means to output the selected access request~~.

72. (Cancelled)

73. (Original) The crossbar switch of claim 65, wherein:

each back end further includes means for receiving and buffering read data from a respective one of the physical memory devices; and

each front end further includes means for receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

74-89. Cancelled.

90-101 (Cancelled)

102. (Currently amended) A crossbar switch, comprising:

means for receiving from a respective device an access request to any one of a plurality of physical memory devices;

means for arbitrating among competing access requests received from any of the means for receiving, selecting one of the competing access requests and forwarding the selected request for implementation on a respective memory device;

wherein the means for arbitrating includes:

a priority generator for each means for receiving capable of generating a composite request priority from a plurality of characteristics of the access requests and a plurality of received operational characteristics;

a priority compare circuit capable of selecting one access request;

a request multiplexer controlled by the priority compare circuit to output the selected access request;

means for merging and interleaving including:

a plurality of programmable registers;

a decode unit receiving the selected request from the request multiplexer to determine whether the selected request is a register operation and, if so, to send a plurality of control and data signals to the registers; and

an output multiplexer for combining register read data with request data for output.

103. (Currently amended) The crossbar switch of claim 102, wherein:

the receiving means includes a plurality of input sorting units~~; or~~

~~the arbitration and selection means includes a plurality of merge and interleave units~~.

104. (Original) The crossbar switch of claim 103, wherein the receiving means further comprises a plurality of translation circuits and wherein each of the input sorting units receives the access requests through a respective one of the Translation circuits.

105. (Original) The crossbar switch of claim 104, wherein each of the translation circuits is capable of receiving an opcode and a virtual address from their respective device, translating the opcode to determine whether the access request is a read or a write, and mapping the virtual address into a physical address, and forwarding the translated opcode and mapped physical address to its respective input sorting unit.

106. (Original) The crossbar switch of claim 102, wherein receiving means furthermore buffers the access requests.

107. (Original) The crossbar switch of claim 106, wherein the receiving means includes a first-in, first-out queue for buffering the access requests.

108. (Original) The crossbar switch of claim 106, wherein each of the input sorting units is capable of stalling its respective device when its buffer is full.

109. (Currently amended) The crossbar switch of claim 102, wherein the ~~arbitration and selection~~ means for arbitrating further includes:

[a] the priority generator for each input sorting unit being further capable of:

receiving [a] the plurality of characteristics for the access request received by the input sorting unit;

receiving [a] the plurality of operational characteristics; and

generating [a] the composite request priority from the characteristics of the access requests and the operational characteristics;

[a] the priority compare circuit being further capable of

comparing the composite request priorities generated by the priority generators; and

selecting the one access request predicated on the comparison of the composite request priorities~~; and~~

~~a request multiplexer controlled by the priority compare circuit to output the selected access request~~.

110. (Cancelled)

111. (Original) The crossbar switch of claim 102, further comprising:

means for receiving and buffering read data from a respective one of the physical memory devices; and

means for receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

112. (Original) The crossbar switch of claim 111, wherein:

the receiving and buffering means includes a plurality of read buffers; or

the receiving and forwarding data includes a plurality of output management units.

113. (Original) The crossbar switch of claim 102, further comprising means for receiving the selected access request from the arbitration and selection means and forwarding the selected access request to a respective one of the physical memory devices.

114. (Original) The crossbar switch of claim 113, wherein the receiving and forwarding means comprises a plurality of memory interfaces.

115-154. (Cancelled)